IN THE CLAIMS

1-20. (Previously Canceled)

21. (Previously Added) An integrated circuit, comprising:

an array of memory cells formed on a substrate; and

a circuit for setting a substrate voltage level, the circuit comprising:

a first n-channel MOSFET having a first gate, a first drain, and a first source, wherein the first gate is coupled to the first drain and the first gate is coupled to a voltage reference level;

a second n-channel MOSFET having a second gate, a second drain, and a second source, wherein the second gate is coupled to the second drain and the second gate is coupled to the first source;

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a third n-channel MOSFET having a third gate, a third drain, and a third source, wherein the third gate is coupled to the third drain and the third drain is coupled to the second source;

a fourth n-channel MOSFET having a fourth gate, a fourth drain, and a fourth source, wherein the fourth gate is coupled to be controlled by a first control voltage and the fourth drain is coupled to the third drain, and the fourth source is coupled to the third source;

a fifth n-channel MOSFET having a fifth gate, a fifth drain, and a fifth source, wherein the fifth gate is coupled to the third gate and the fifth drain is coupled to the third source and the fifth source is coupled to the substrate; and

a sixth n-channel MOSFET having a sixth gate, a sixth drain, and a sixth source, wherein the sixth drain is coupled to the fifth drain and the sixth source is coupled to the fifth source and the sixth gate is coupled to be controlled by a second control voltage.

22. (Previously Added) The integrated circuit of claim 19, wherein the plurality of switches comprises a plurality of bypass transistors.

23. (Previously Added) The integrated circuit of claim 19 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit such that the one diode is bypassed during normal operation but can be selectively unbypassed during testing operations.

24. (Previously Added) An integrated circuit, comprising:

an array of memory cells formed on a substrate;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level;

wherein the substrate voltage regulator circuit comprises a series of diodes coupled between a supply voltage source and the substrate; and

wherein the substrate voltage regulator circuit comprises at least one bypass transistor coupled to at least one diode in the series of diodes for electrically bypassing at least one diode.

c1 cont.

25. (Previously Added) The integrated circuit of claim 24 wherein the substrate voltage regulator circuit includes a plurality of bypass transistors, each one of the plurality of bypass transistors coupled to at least one diode in the series of diodes for electrically bypassing a plurality of diodes.

26. (Previously Added) The integrated circuit of claim 24 wherein at least one bypass transistor is coupled to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

27. (Previously Added) The integrated circuit of claim 24 wherein the at least one bypass transistor is turned off during normal operation of the integrated circuit such that at least one diode is unbypassed during normal operation but can be selectively bypassed during testing operations.

28. (Previously Added) The integrated circuit of claim 24 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit such that at least one diode is bypassed during normal operation but can be selectively unbypassed during testing operations.

29. (Previously Added) An integrated circuit, comprising:

an array of memory cells formed on a substrate;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level;

wherein the substrate voltage regulator circuit comprises a series of diodes coupled between a supply voltage source and the substrate; and

wherein the substrate voltage regulator circuit comprises at least one bypass transistor coupled to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

C1 Cont.

30. (Previously Added) The integrated circuit of claim 29 wherein the at least one bypass transistor is turned off during normal operation of the integrated circuit such that at least one diode is unbypassed during normal operation but can be selectively bypassed during testing operations.

31. (Previously Added) The integrated circuit of claim 29 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit such that at least one diode is bypassed during normal operation but can be selectively unbypassed during testing operations.

32. (Previously Added) An integrated circuit, comprising:

an array of memory cells formed on a substrate;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level;

wherein the substrate voltage regulator circuit comprises a series of diodes coupled between a supply voltage source and the substrate; and

wherein the substrate voltage regulator circuit comprises a plurality of bypass transistors coupled to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

33. (Previously Added) The integrated circuit of claim 32 wherein the at least one bypass transistor is turned off during normal operation of the integrated circuit such that at least one diode is unbypassed during normal operation but can be selectively bypassed during testing operations.

34. (Previously Added) The integrated circuit of claim 32 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit such that at least one diode is bypassed during normal operation but can be selectively unbypassed during testing operations.

C1 cont.

35. (Previously Added) An integrated circuit, comprising:

an array of memory cells formed on a substrate;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level, the substrate voltage regulator circuit comprising a series of diode connected transistors coupled between a supply voltage source and the substrate, and at least one bypass transistor coupled to at least one diode connected transistor in the series of diode connected transistors for electrically bypassing at least one diode connected transistor,

each diode connected transistor of the series of diode connected transistors has a junction voltage drop, and the substrate voltage bias level is defined by a supply voltage level minus junction voltage drops of unbypassed diode connected transistors of the series of diode connected transistors.

36. (Previously Added) The integrated circuit of claim 35 wherein the at least one bypass transistor is coupled to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

37. (Previously Added) The integrated circuit of claim 35 wherein the at least one bypass transistor is turned off during normal operation of the integrated circuit such that at least one diode is unbypassed during normal operation but can be selectively bypassed during testing operations.

38. (Previously Added) The integrated circuit of claim 35 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit such that at least one diode is bypassed during normal operation but can be selectively unbypassed during testing operations.

39. (Previously Added) An integrated circuit, comprising:

an array of memory cells formed on a substrate;

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a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level, the substrate voltage regulator circuit comprising a series of diode connected transistors coupled between a supply voltage source and the substrate, and at least one bypass transistor coupled to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors,

each diode connected transistor of the series of diode connected transistors has a junction voltage drop, and the substrate voltage bias level is defined by a supply voltage level minus junction voltage drops of unbypassed diode connected transistors of the series of diode connected transistors.

40. (Previously Added) The integrated circuit of claim 39 wherein the substrate voltage regulator circuit includes a plurality of bypass transistors, each one of the plurality of bypass transistors coupled to at least one diode connected transistor in the series of diode connected transistors for electrically bypassing a plurality of diode connected transistors.

41. (Previously Added) The integrated circuit of claim 39 wherein the at least one bypass transistor is turned off during normal operation of the integrated circuit memory device such that the one diode connected transistor is unbypassed during normal operation but can be selectively bypassed during testing operations.

42. (Previously Added) The integrated circuit of claim 39 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit memory device such that

the one diode connected transistor is bypassed during normal operation but can be selectively unbypassed during testing operations.

43. (Previously Added) An integrated circuit, comprising:

an array of memory cells formed on a substrate;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level, the substrate voltage regulator circuit comprising a series of diode connected transistors coupled between a supply voltage source and the substrate, and a plurality of bypass transistors coupled to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors,

each diode connected transistor of the series of diode connected transistors has a junction voltage drop, and the substrate voltage bias level is defined by a supply voltage level minus junction voltage drops of unbypassed diode connected transistors of the series of diode connected transistors.

44. (Previously Added) The integrated circuit of claim 43 wherein the plurality of bypass transistors is turned off during normal operation of the integrated circuit memory device such that the one diode connected transistor is unbypassed during normal operation but can be selectively bypassed during testing operations.

45. (Previously Added) The integrated circuit of claim 43 wherein the plurality of bypass transistors is turned on during normal operation of the integrated circuit memory device such that the one diode connected transistor is bypassed during normal operation but can be selectively unbypassed during testing operations.